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WHAT IS CLAIMED IS:

1. A processing unit, comprising:

a plurality of subcircuits;

circuitry for generating a clock signal to said plurality of subcircuits;

circuitry for detecting the assertion of a control signal; and

circuitry coupled to said detecting circuitry for disabling the clock signal to ones of said subcircuits responsive to said control signal.

2. The processing unit of Claim 1 wherein said disabling circuitry comprises circuitry for maintaining the clock signal to said ones of said subcircuits in a predetermined state.

3. The processing unit of Claim 1 and further comprising circuitry for generating an acknowledge signal indicating that the clock signal to said ones of said subcircuits has been disabled.

4. The processing unit of Claim 1 wherein said disabling circuitry comprises circuitry for executing instructions currently in one or more of said subcircuits prior to disabling said ones of said subcircuits.

5. The processing unit of Claim 4 wherein said one or more subcircuits comprise a microcode memory and an execution unit.

6. The processing unit of Claim 1 and further comprising circuitry for resuming the clock signal to said ones of said subcircuits responsive to de-assertion of said control signal.

7. The processing unit of Claim 1 and further comprising circuitry for generating an interrupt responsive to detecting assertion of said control signal.

8. The processing unit of Claim 7 and further comprising an exception processor for executing a microcode routine responsive to said interrupt.

9. A computer comprising:
a processing unit comprising;
a plurality of subcircuits;
circuitry for generating a clock signal to said plurality of subcircuits;
circuitry for detecting the assertion of a control signal; and
circuitry coupled to said detecting circuitry for disabling the clock signal to ones of said subcircuits responsive to said control signal;
circuitry for detecting conditions for suspending operations of said processing unit and asserting said control signal responsive thereto; and
circuitry for detecting conditions for resuming operation of said processing unit and de-asserting said control signal responsive thereto.

10. The computer of Claim 9 and further comprising a display for outputting data.

11. The computer of Claim 10 and further comprising circuitry for disabling said display.

12. The computer of Claim 10 and further comprising a coprocessor coupled to said processing unit.

13. The computer of Claim 9 wherein said disabling circuitry comprises circuitry for disabling the clock signals to said ones of said subcircuits after said executing instructions in one or more of said subcircuits.

14. The computer of Claim 9 wherein said processing unit further comprises circuitry for resuming the clock signal to said ones of said subcircuits responsive to de-assertion of said control signal.

15. The computer of Claim 9 wherein said processing unit further comprises circuitry for generating an acknowledge signal indicating that the clock signal to said ones of said subcircuits has been disabled.

16. A method of conserving power consumed by a processing unit comprising the steps of:

generating a clock signal to a plurality of subcircuits;

detecting the assertion of a control signal;

disabling the clock signal to ones of said subcircuits responsive to said control signal.

17. The method of Claim 16 wherein said disabling step comprises the step of maintaining the clock signal to said ones of said circuits in a predetermined state.

18. The method of Claim 16 and further comprising the step of generating an acknowledge signal indicating that the clock signal to said ones of said subcircuits has been disabled.

19. The method of Claim 16 wherein said disabling step comprises disabling the clock signal to said ones of said subcircuits after said executing instructions in ones of said subcircuits.

20. The method of Claim 16 and further comprising the step of resuming the clock signal to said ones of said subcircuits responsive to de-assertion of said control signal.

21. The method of Claim 16 and further comprising the steps of generating an interrupt responsive to detecting said control signal.

22. The method of Claim 21 and further comprising the step of executing a microcode routine responsive tc said interrupt.